I claim:

1. A process for re-use of a silicon wafer having two major, generally parallel surfaces, one being the front surface of the wafer and the other being the back surface of the wafer, a circumferential edge joining the front and back surfaces, a central axis, a radius extending from the central axis to the circumferential edge of at least about 75 mm, a central plane approximately equidistant between the front and back surfaces, and a precipitate free zone having a thickness of at least 20 micrometers adjacent the front surface, the process comprising:

(a) subjecting the wafer to an oxide growth step to form an oxide layer having a thickness greater than 2 nanometers,

(b) after step (a), thinning the wafer by removing material from substantially the entire front surface to provide a thinned wafer having a thinned precipitate free zone, and

(c) polishing the front surface of the thinned wafer to a specular finish.

2. The process of claim 1 wherein the thickness of the thinned and polished wafer is at least about 10 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

3. The process of claim 1 wherein the precipitate free zone, prior to said oxide growth step had a thickness of at least about 30 micrometers.

4. The process of claim 3 wherein the thickness of the thinned and polished wafer is at least about 15 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

5. The process of claim 1 wherein the precipitate free zone, prior to said oxide growth step had a thickness of at least about 50 micrometers.

6. The process of claim 5 wherein the thickness of the thinned and polished wafer is at least about 30 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

7. The process of claim 1 wherein the thickness of the thinned and polished wafer is at least about 15 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

8. The process of claim 1 wherein the thickness of the thinned and polished wafer is at least about 30 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

9. The process of claim 1 wherein the precipitate free zone extends from the front surface to the back surface of the wafer.

10. The process of claim 9 wherein the thickness of the thinned and polished wafer is at least about 10

micrometers thinner than the thickness of the wafer prior to the oxide growth step.

11. The process of claim 9 wherein the thickness of the thinned and polished wafer is at least about 15 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

12. The process of claim 9 wherein the thickness of the thinned and polished wafer is at least about 30 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

13. The process of claim 1 wherein, prior to said oxidation step, the wafer contained oxygen precipitate nucleation centers between the central plane and the precipitate free zone.

14. The process of claim 1 wherein the wafer further comprises a first axially symmetric region which is substantially free of agglomerated intrinsic point defects.

15. The process of claim 14 wherein the first axially symmetric region is a region in which vacancies are the predominant intrinsic point defect.

16. The process of claim 15 wherein the wafer further comprises a second axially symmetric region in which silicon self-interstitial atoms are the predominant intrinsic point

defect and which is substantially free of agglomerated silicon self-interstitial intrinsic point defects.

17. The process of claim 1 wherein the polished wafer is used as a monitor wafer in at least one step of a semiconductor device fabrication process.

18. The process of claim 1 wherein a semiconductor device is formed in the device layer of the polished wafer.

19. The process of claim 1 wherein prior to step (a), the wafer has a non-uniform distribution of crystal lattice vacancies with the peak concentration of vacancies being at a maximum at a distance of at least 20 micrometers from the front surface of the wafer.

20. The process of claim 1 wherein prior to step (a), the wafer has a non-uniform distribution of crystal lattice vacancies with the peak concentration of vacancies being at a maximum at a distance of at least 30 micrometers from the front surface of the wafer.

21. The process of claim 1 wherein prior to step (a), the wafer has a non-uniform distribution of crystal lattice vacancies with the peak concentration of vacancies being at a maximum at a distance of at least 40 micrometers from the front surface of the wafer.

22. The process of claim 1 wherein prior to step (a), the wafer has a non-uniform distribution of crystal lattice

vacancies with the peak concentration of vacancies being at a maximum at a distance of at least 50 micrometers from the front surface of the wafer.

23. The process of claim 1 wherein the wafer has a concentration of oxygen which is less than 9 PPMA.

24. The process of claim 1 wherein the wafer has a concentration of oxygen which is less than 8 PPMA.

25. The process of claim 1 wherein an oxide layer having a thickness of at least 3 nanometers is grown on the front surface of the wafer in step (a).

26. The process of claim 1 wherein an oxide layer having a thickness of at least 25 nanometers is grown on the front surface of the wafer in step (a).

27. The process of claim 1 wherein an oxide layer having a thickness of at least 50 nanometers is grown on the front surface of the wafer in step (a).

28. A process for re-use of a silicon wafer having two major, generally parallel surfaces, one being the front surface of the wafer and the other being the back surface of the wafer, a circumferential edge joining the front and back surfaces, a central axis, a radius extending from the central axis to the circumferential edge of at least about 75 mm, a central plane approximately equidistant between the front and back surfaces, and a precipitate free zone

adjacent the front surface which is free of oxygen precipitate nucleation centers to a known or predetermined depth, the process comprising:

(a) growing an oxide layer having a thickness of at least 2 nanometers on the front surface thereof,

(b) after step (a), thinning the wafer by removing material from substantially the entire front surface to provide a thinned wafer having a thinned precipitate free zone, wherein said thinning is designed to provide a thinned precipitate free zone having a thickness of at least 5 micrometers, and

(c) polishing the front surface of the thinned wafer to a specular finish.

29. The process of claim 28 wherein the precipitate free zone, prior to said oxide growth step had a thickness of at least about 20 micrometers.

30. The process of claim 29 wherein the thickness of the thinned and polished wafer is at least about 10 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

31. The process of claim 28 wherein the precipitate free zone, prior to said oxide growth step had a thickness of at least about 30 micrometers.

32. The process of claim 31 wherein the thickness of the thinned and polished wafer is at least about 15

micrometers thinner than the thickness of the wafer prior to the oxide growth step.

33. The process of claim 28 wherein the precipitate free zone, prior to said oxide growth step had a thickness of at least about 50 micrometers.

34. The process of claim 33 wherein the thickness of the thinned and polished wafer is at least about 30 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

35. The process of claim 28 wherein the thickness of the thinned and polished wafer is at least about 10 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

36. The process of claim 28 wherein the thickness of the thinned and polished wafer is at least about 15 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

37. The process of claim 28 wherein the thickness of the thinned and polished wafer is at least about 30 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

38. The process of claim 28 wherein the precipitate free zone extends from the front surface to the back surface of the wafer.

39. The process of claim 38 wherein the thickness of the thinned and polished wafer is at least about 10 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

40. The process of claim 38 wherein the thickness of the thinned and polished wafer is at least about 15 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

41. The process of claim 38 wherein the thickness of the thinned and polished wafer is at least about 30 micrometers thinner than the thickness of the wafer prior to the oxide growth step.

42. The process of claim 28 wherein, prior to said oxidation step, the wafer contained oxygen precipitate nucleation centers between the central plane and the precipitate free zone.

43. The process of claim 28 wherein the wafer further comprises a first axially symmetric region which is substantially free of agglomerated intrinsic point defects.

44. The process of claim 43 wherein the first axially symmetric region is a region in which vacancies are the predominant intrinsic point defect.

45. The process of claim 44 wherein the wafer further comprises a second axially symmetric region in which silicon self-interstitial atoms are the predominant intrinsic point defect and which is substantially free of agglomerated silicon self-interstitial intrinsic point defects.

46. The process of claim 28 wherein the polished wafer is used as a monitor wafer in at least one step of a semiconductor device fabrication process.

47. The process of claim 28 wherein a semiconductor device is formed in the device layer of the polished wafer.

48. The process of claim 28 wherein prior to step (a), the wafer has a non-uniform distribution of crystal lattice vacancies with the peak concentration of vacancies being at a maximum at a distance of at least 20 micrometers from the front surface of the wafer.

49. The process of claim 28 wherein prior to step (a), the wafer has a non-uniform distribution of crystal lattice vacancies with the peak concentration of vacancies being at a maximum at a distance of at least 30 micrometers from the front surface of the wafer.

50. The process of claim 28 wherein prior to step (a), the wafer has a non-uniform distribution of crystal lattice vacancies with the peak concentration of vacancies being at a maximum at a distance of at least 40 micrometers from the front surface of the wafer.

51. The process of claim 28 wherein prior to step (a), the wafer has a non-uniform distribution of crystal lattice vacancies with the peak concentration of vacancies being at a maximum at a distance of at least 50 micrometers from the front surface of the wafer.

52. The process of claim 28 wherein the wafer has a concentration of oxygen which is less than 10 PPMA.

53. The process of claim 28 wherein the wafer has a concentration of oxygen which is less than 9 PPMA.

54. The process of claim 28 wherein an oxide layer having a thickness of at least 3 nanometers is grown on the front surface of the wafer in step (a).

55. The process of claim 28 wherein an oxide layer having a thickness of at least 25 nanometers is grown on the front surface of the wafer in step (a).

56. The process of claim 28 wherein an oxide layer having a thickness of at least 50 nanometers is grown on the front surface of the wafer in step (a).

57. A process for the preparation of a silicon wafer having two major, generally parallel surfaces, one being the front surface of the wafer and the other being the back surface of the wafer, a circumferential edge joining the front and back surfaces, a central axis, a radius extending

from the central axis to the circumferential edge of at least about 75 mm, a central plane approximately equidistant between the front and back surfaces, and a non-uniform distribution of crystal lattice vacancies with the maximum concentration of vacancies being at a distance, D, from the front surface, the process comprising:

thinning the wafer by removing material from the front surface to provide a thinned wafer, the amount of material removed from the front surface being insufficient to reach said distance, D, and

polishing the front surface of the thinned wafer to a specular finish.

58. The process of claim 57 wherein D is at least 20 micrometers.

59. The process of claim 57 wherein D is at least 30 micrometers.

60. The process of claim 57 wherein D is at least 40 micrometers.

61. The process of claim 60 wherein said thinning reduces the thickness of the wafer by at least 20 micrometers.

62. The process of claim 60 wherein said thinning reduces the thickness of the wafer by at least 30 micrometers.

63. The process of claim 57 wherein D is at least 50 micrometers.

64. The process of claim 63 wherein said thinning reduces the thickness of the wafer by at least 20 micrometers.

65. The process of claim 63 wherein said thinning reduces the thickness of the wafer by at least 30 micrometers.

66. The process of claim 57 wherein said thinning reduces the thickness of the wafer by at least 20 micrometers.

67. The process of claim 57 wherein said thinning reduces the thickness of the wafer by at least 30 micrometers.

68. The process of claim 57 wherein prior to said thinning, an oxide layer having a thickness of at least 2 nanometers is grown on the front surface of the wafer.

69. The process of claim 68 wherein D is at least 20 micrometers.

70. The process of claim 68 wherein D is at least 30 micrometers.

71. The process of claim 68 wherein D is at least 40 micrometers.

72. The process of claim 71 wherein said thinning reduces the thickness of the wafer by at least 20 micrometers.

73. The process of claim 71 wherein said thinning reduces the thickness of the wafer by at least 30 micrometers.

74. The process of claim 68 wherein D is at least 50 micrometers.

75. The process of claim 74 wherein said thinning reduces the thickness of the wafer by at least 20 micrometers.

76. The process of claim 74 wherein said thinning reduces the thickness of the wafer by at least 30 micrometers.

77. The process of claim 68 wherein said thinning reduces the thickness of the wafer by at least 20 micrometers.

78. The process of claim 68 wherein said thinning reduces the thickness of the wafer by at least 30 micrometers.

79. The process of claim 57 wherein prior to said thinning, an oxide layer having a thickness of at least 3 nanometers is grown on the front surface of the wafer.

80. The process of claim 57 wherein prior to said thinning, an oxide layer having a thickness of at least 25 nanometers is grown on the front surface of the wafer.

81. The process of claim 57 wherein prior to said thinning, an oxide layer having a thickness of at least 50 nanometers is grown on the front surface of the wafer.